(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 260 858 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 87307897.6

(51) Int. Cl.⁴: H01L 31/10 , H01L 27/14

(22) Date of filing: 07.09.87

(30) Priority: 19.09.86 JP 219668/86

(43) Date of publication of application:
23.03.88 Bulletin 88/12

(84) Designated Contracting States:
DE FR GB IT NL

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(54) Photoelectric conversion apparatus.

(57) A photoelectric conversion apparatus comprising a plurality of photoelectric conversion cells, each including a semiconductor transistor having a control electrode area which in turn includes a plurality of main electrode areas for reading signals, wherein the potential of the control electrode area is controlled to store carriers produced by optical pumping in the control electrode area, to read, from the main electrode area, a signal controlled by the storage voltage produced due to the storage, and to perform a refreshing operation to nullify the carriers stored in the control electrode area. A device is provided for performing a peak detection on the basis of signals from the main electrode area. At least one of the photoelectric conversion cells is shielded from light. The peak detection device performs the peak detection by detecting the difference between a peak signal obtained on the basis of a signal from the photoelectric conversion cells and a dark signal from the photoelectric conversion cells shielded from light.

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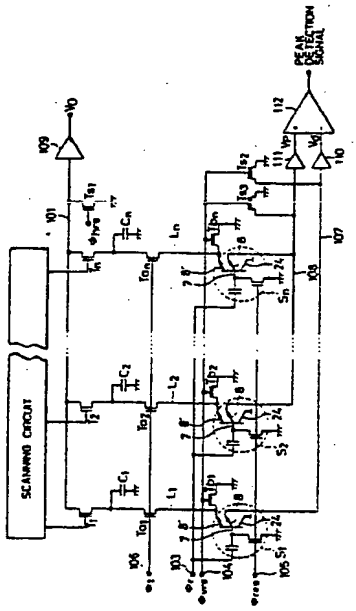


FIG. 4

Photoelectric Conversion Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to a photoelectric conversion apparatus. An embodiment of the apparatus includes a plurality of photoelectric conversion cells each including a transistor having a control electrode area, wherein the potential of the control electrode area of each transistor is controlled a store carriers produced by optical pumping in the control electrode area, to read the stored voltage, and to nullify the stored carriers. An embodiment of the photoelectric conversion apparatus is intended to perform a precise peak detection.

Related Background Art

Fig. 1A is a schematic plan view of one example of a photoelectric conversion cell described in Japanese Patent Application No. 252653/1985, Fig. 1B is a cross sectional view taken along the line A-A of Fig. 1A and Fig. 1C is an equivalent circuit diagram of the cell.

In these Figures, an n-silicon substrate 1 has an n^--epitaxial layer 3 formed thereon which has a p-base area 4 formed thereon which has n^+-emitter areas 5 and 5' formed thereon. The emitter areas 5 and 5' are connected to emitter electrodes 8 and 8', respectively.

In this example, an insulating area 14 and the underlying n^+-area 15 constitute a device separating area 2 which separates adjacent photoelectric conversion cells from each other.

Formed on p-base area 4 is an oxide film 6 on which is formed a capacitor electrode 7 with an insulating film 16 thereon. Formed on film 16 is a light shielding film 17 which shields from light the area on which the capacitor electrode and emitter electrode are formed with a photosensitive surface being formed in the main portion of p-base area 4. A protective insulating film 18 is formed on the light shielding film 17 and the insulating film 16 portion constituting the light-sensitive face.

In the basic operation, first assume that the p-base area 4 which is the base of a bipolar transistor is in an initial negative-potential state. When light enters the photosensitive face of this p-base area 4, electron-positive hole pairs will be produced, the positive holes of which are stored in p-base area 4, which changes the potential of p-base area 4 in the positive-going sense (storage operation).

Subsequently, a positive read voltage pulse is applied to capacitor electrode 7 and a read signal, namely, optical information, corresponding to a change in the base potential during storage operation is output from emitter electrodes 8 and 8' in a floating state (read operation). At this time, the quantity of electric charges stored in p-base area 4 does not virtually decrease, so that non-destructive reading is possible.

In order to eliminate the positive holes stored in p-base area 4, emitter electrode 8 is grounded and a positive refresh pulse voltage is applied to capacitor electrode 7. This biases p-base area 4 forwardly relative to n^+-emitter areas 5 and 5' to thereby eliminate the positive holes stored. When the refresh pulse falls down, p-base area 4 returns to its initial negative-potential state (refresh operation). Thereafter, similarly, storage, read and refresh operations are repeated.

Such double-emittered photoelectric conversion cell allows a signal to be read from either of both the emitters, so that the mean value or peak value can be easily taken using one signal and light measurement and/or peak value detection can be performed in parallel with the signal reading.

Fig. 2 is a circuit diagram showing one example of a photoelectric conversion apparatus using cells described in the above Patent Application No. 252653/1985. In Fig. 2, double-emitter photoelectric conversion cells S1-Sn are arranged in a line. Emitter electrodes 8 are connected to an output line 101 via vertical lines L1-Ln and transistors T1-Tn. Respective signals are read serially to signal output line 101, amplified by amplifiers and output outside as an output signal VO.

On the other hand, emitter electrodes 8' are connected to a common line 102, so that the peak values Vp of respective signals appear on the common line 102. The use of peak values Vp allows adjustment of the gain of the signal output amplifier and the durations of storage in the photoelectric conversion cells. Further, peak value detection is possible at the same time as reading from the emitter electrodes 8, so that the image pickup operation is speeded up.

However, according to the conventional photoelectric conversion apparatus, noise components due to a dark current in the photoelectric conversion cell are contained in the output signal, so that apparatus has the problem that the peak value Vp does not correspond accurately to the peak signal in the photoelectric conversion cell.

SUMMARY OF THE INVENTION

In order to solve the above problems, a photoelectric conversion apparatus according to an embodiment of this invention comprises:

a plurality of photoelectric conversion cells, each including a semiconductor transistor having a control electrode area which in turn includes a plurality of main electrode areas for reading signals, wherein the potential of the control electrode area of each cell is controlled to store carriers produced by optical pumping in the control electrode area, to read, from the main electrode area, a signal controlled by the storage voltage produced due to the storage, and to perform a refreshing operation to nullify the carriers stored in the control electrode area;

means for performing a peak detection on the basis of signals from the main electrode area; and

at least one of the photoelectric conversion cells being shielded from light whereby the peak detection is performed by detecting the difference between a peak signal obtained on the basis of a signal from the photoelectric conversion cells and a dark signal from the photoelectric conversion cells shielded from light.

By using the dark signal in the photoelectric conversion cell shielded from light as mentioned above, noise components due to the dark signal are eliminated from the peak singal obtained from the signal in the photoelectric conversion cell to thereby allow correct peak detection.

A photoelectric conversion cell shielded from light and a photoconductive conversion cell not shielded from light are referred hereinafter as to the shielded-from-light bit and the open bit, respectively.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1A is a schematic plan view of one example of a photoelectric conversion cell described in Japanese Patent Application No. 252653/1985.

Fig. 1B is a cross-sectional view taken along the line A-A of Fig. 1A;

Fig. 1C is an equivalent circuit diagram of the cell;

Fig. 2 is a circuit diagram showing one example of a conventional photoelectric conversion apparatus;

Fig. 3A is a schematic plan view of a photoelectric conversion cell used in one embodiment of a photoelectric conversion apparatus according to this invention;

Fig. 3B is a cross-sectional view taken along the line A-A of Fig. 3A;

Fig. 3C is an equivalent circuit diagram of the cell of Fig. 3A;

Fig. 4 is a circuit diagram of the first embodiment of a photoelectric conversion apparatus according to this invention;

Fig. 5 is a circuit diagram of a second embodiment of this invention; and

Fig. 6 is a schematic of one example of an image pickup apparatus using the above embodiment.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of this invention will now be described in more detail with reference to the drawings. First the structure and basic operation of a photoelectric conversion cell used in the embodiments will now be described.

Fig. 3A is a schematic plan view of a photoelectric conversion cell used in one embodiment of a photoelectric conversion apparatus according to this invention. Fig. 3B is a cross-sectional view taken along the line A-A of Fig. 3A. Fig. 3C is an equivalent circuit diagram of the cell. Like reference numerals are used to denote like areas and members in Figs. 1 and 3. In Fig. 3, n^--epitaxial layer 3 has p-base area 4 formed thereon which in turn has n^+ emitter areas 5 and 5' formed thereon.

Formed on p-base area 4 is oxide film 6 on which a capacitor electrode 7 is formed. Formed on n^--epitaxial layer 3 is oxide film 6 on which a reset MOS transistor gate electrode 22 is formed. Capacitor and gate electrodes 7 and 22 are formed of polysilicon. P^+-areas 20 and 21 which are the source and drain areas of the reset MOS transistor are formed in a self-aligning manner with p^+-area 20 being joined to p-base area 4 and with p^+-area 21 having an Al electrode 28 connected thereto.

Formed on oxide film 6 is an inter-layer insulating layer 25 through which emitter electrodes 8 and 8' are connected to n^+-areas 5 and 5', respectively. Formed on oxide film 6 is a collector electrode 24 which is connected through n^+-area 23 to n^--epitaxial layer 3 which is the collector area. Further, a passivation film 26 covers the insulating layer 25, emitter electrodes 8 and 8' and collector electrode 24.

In the case of the photoelectric conversion cell shielded from light, inter-insulating layer 25 has an insulating layer formed thereon on which insulating layer a shielded-from-light layer is formed. A passivation layer 26 is formed on the insulating layer 25, the emitter and collector electrodes.

The operation of the photoelectric conversion cell having such structure is basically the same as that of the prior art except that provision of the reset MOS transistor results in a refreshing operation at a higher speed than the prior art one. Namely, when a desired voltage is applied to the electrode 28 of the reset MOS transistor, and the refreshing operation is performed, first, the reset MOS transistor is turned on which maintains the potential of p-base area 4 constant irrespective of the storage voltage. Thereafter, a refreshing pulse is applied to capacitor electrode 7 to thereby eliminate completely the carriers stored in p-base area 4 at high speeds.

Fig. 4 is a circuit diagram of a first embodiment of a photoelectric conversion apparatus according to this invention. In Fig. 4, the shielded-from-light bit S1 and open bits S2-Sn, each including the above photoelectric conversion cell, are arranged.

Capacitor electrodes 7 of the respective bits are connected together to a terminal 103 with a constant positive voltage being applied to collector electrodes 24. The electrodes 28 of the reset MOS transistors are grounded with gate electrodes 22 being connected together to a terminal 105.

Emitter electrodes 8' of the respective bits are connected to corresponding vertical lines L1-Ln which are connected via transistors Ta1-Tan to corresponding electric charge storage capacitors C1-Cn and via corresponding transistors T1-Tn to an output signal line 101. Output signal line 101 is grounded via a reset transistor Ts1 and also connected to an amplifier 109. The gate electrodes of transistors T1-Tn are connected to parallel output terminals of a scanning circuit and sequentially turned on in accordance with the scanning circuit.

Vertical lines L1-Ln are grounded via corresponding transistors Tb1-Tbn, the gate electrodes of which are connected together to a terminal 104. Emitter electrode 8 of shielded-from-light bit S1 is connected to a line 107 which is grounded via a transistor Ts2 and connected to an amplifier 110.

The respective emitter electrodes 8 of open bits S2-S2n are connected together to a line 108 which is grounded via a transistor Ts3 and also connected to an amplifier 111.

The respective gate electrodes of transistors Ts2 and Ts3 are connected to a terminal 104. The output terminal of amplifiers 110 and 111 are connected to input terminals of a differential amplifier 112. The operation of this embodiment will now be explained.

Refreshing Operation

First, a signal Øres is applied to terminal 105 to turn on the respective reset MOS transistors of the bits to thereby maintain the p-base areas 4 of all the bits at constant potential. Subsequently, a signal Øvrs is applied to terminal 104 to turn on transistors Tb1-Tbn, Ts2 and Ts3 to thereby ground the emitter electrodes 8 and 8' of all the bits. A refreshing pulse Ør is then applied to terminals 103 to eliminate the carriers stored in p-base area 4, as described above. It is to be noted that before these operations, the reset MOS transistors of the bits should be turned off.

Storage Operation

After a falling edge of the refreshing pulse Ør, carriers corresponding to the illuminations of the respective light beams start to be stored in the respective p-base areas 4 of the open bits.

Read Operation

Thereafter, when a storage time T designated by a control unit 304 of Fig. 6 has passed, first, transistors Tb1-Tbn, Ts2 and Ts3 are turned off and the emitter electrodes 8 and 8' of the respective bits are rendered floating.

Subsequently, a signal Øt is applied to terminal 106 to turn on transistors Ta1-Tan and a read pulse is applied to terminal 103. Storage time T is from the falling edge of the pulse Ør to the rising edge of the read pulse Øt. A dark signal is thereby read from the shielded-from-light bit to vertical line L1 and stored in capacitor C1, and signals are read from the respective open bits to the corresponding vertical lines L2-Ln and stored in the corresponding capacitors C2-Cn.

Subsequently, transistors Ta1-Tan are turned off, transistors T1-Tn are then sequentially turned on by the scanning circuit to read signals sequentially to output signal line 101 to thereby output the signals via amplifier 109. At this time, each time a signal is output, signal Øhrs turns on transistor Ts1 to refresh the remaining charges on output line 101.

Peak Detection

In parallel with the above read operation, the peak detection is formed. When a read pulse is applied to terminal 103 during reading operation, a dark signal is read from the shielded-from-light bit to line 107, signals are read from the open bits to

lines 108. Since lines 108 are connected in common, the peak value of signals from the open bits S2-Sn appears on lines 108. Therefore, amplifiers 110 and 111 output a dark signal Vd and a peak signal Vp, respectively, and differential amplifier 112 calculates the difference |Vp - Vd| between these signals to thereby provide a peak detection signal free from noise components due to the dark signal.

Fig. 5 is a circuit diagram of a second embodiment of this invention. Like reference numerals are used to denote like circuit blocks or elements in the first and second embodiments.

In Fig. 5, the emitter electrode 8' of the shielded-from-light bit S1 is connected to a charge storage capacitor C1 and a line 107 via a vertical line L1 and a transistor Ta1. Therefore, as in other open bits, a dark signal from the shielded-from-light bit is stored in capacitor C1 during read operation and amplified by amplifier 110 and output as a dark signal Vd.

Emitter electrode 8 of shielded-from-light bit S1 is connected to a line 108 together with the respective emitter electrodes 8 of the open bits S2-Sn.

As mentioned above, since the circuit structure of emitter electrodes 8 and 8' of shielded-from-light bit S1 is similar to that of the open bits S2-Sn, the base parasitic capacitance of the shielded-from-light bit S1 becomes the same as that of other open bits, and since the emitter electrodes 8 of all the bits are connected to line 108, the quantities of feedback from the emitter electrodes 8 are equal for all the bits.

As a result, although the storage time and temperature change, no relative fluctuations in signal output between shielded-from-light bit S1 and open bits S2-Sn will not be produced. Therefore, a dark signal from shielded-from-light bit S1 becomes a stabilized reference in peak detection and the calculation of the difference |Vp - Vd| between both the signals by differential amplifier 112 provides a further precise peak detection compared to the first embodiment.

While the above respective embodiments have been described for a line sensor, of course, area sensors may be similarly constructed to obtain similar effects. While in the above embodiment, only a single shielded-from-light bit is shown as being used, a plurality of shielded-from-light bits may be used as needed.

Fig. 6 is a schematic of one example of an image pickup device using the above embodiment. In Fig. 6, an image pickup device 301 may have the structure of each of the above embodiments. The output signal V0 of image pickup device 301 is subjected to a processing such as gain adjustment by a signal processing circuit 302 and output as a standard television signal such as an NTSC signal.

A driver 303 supplies various pulses ∅ to a drive image pickup device 301 and operates under the control of control unit 304. The peak detection signal output from a differential amplifier 112 of image pickup device 301 is input to control unit 304 which controls the gain of the signal processing circuit 302, the storage time of image pickup device 301 and an exposure control means 305 so that a signal level formed by image pickup device 301 becomes optimal.

As described above, the present embodiments are capable of correct peak detection, and performing an appropriate image pickup.

As described above in detail, the photoelectric conversion apparatus according to this invention utilizes a dark signal from a photoelectric conversion cell shielded from light to eliminate noise components from a peak signal based on a signal from the photoelectric conversion cell to thereby provide correct peak detection.

Claims

1. A photoelectric conversion apparatus comprises:
a plurality of photoelectric conversion cells, each including a semiconductor transistor having a control electrode area which in turn includes a plurality of main electrode areas for reading signals, wherein the potential state of the control electrode area of each cell is controlled to store carriers produced by optical pumping in the control electrode area, to read, from the main electrode area, a signal controlled by the storage voltage produced due to the storage, and to perform a refreshing operation to nullify the carriers stored in the control electrode area;
at least one of the photoelectric conversion cells being shielded from light; and
means for performing a peak detection by detecting the difference between a peak signal obtained on the basis of a signal from the main electrode areas of the photoelectric conversion cells and a dark signal from the photoelectric conversion cells shielded from light.

2. A photoelectric conversion apparatus of claim 1, wherein each such photoelectric conversion cell includes two main electrode areas for reading signals, one main electrode area of the photoelectric conversion cells shielded from light and one main electrode area of each of the photoelectric conversion cells not shielded from light being connected together to a common line, the peak detection being performed by sensing the difference between a signal appearing on the com-

mon line and a signal from the other electrode area of the photoelectric conversion cells shielded from light.

3. A photoelectric conversion apparatus of claim 1, wherein each such semiconductor transistor includes a bipolar transistor.

4. A photoelectric conversion apparatus of claim 1, further including:
control means for controlling the output level of the photoelectric conversion cells to an appropriate one using the output of the peak detection performing means.

5. A photoelectric conversion apparatus of claim 4, wherein the control means includes means for controlling exposure to the photoelectric conversion cells.

6. A photoelectric conversion apparatus of claim 4, wherein the control means includes means for controlling a signal storage time in the photoelectric conversion cells.

7. A photoelectric conversion apparatus of claim 4, wherein the control means includes means for controlling the gain of the output from the photoelectric conversion cells.

8. A photoelectric conversion apparatus comprising:

a) a plurality of photoelectric conversion cells, each including at least a first and a second output terminal, the cells including ones shielded from light and exposed to light; and

b) means for performing a calculation between at least signals at the first output terminals of the exposed cells and a signal at one output terminal of the cell shielded from light.

9. A photoelectric conversion apparatus of claim 8, wherein the photoelectric conversion cells include a transistor.

10. A photoelectric conversion apparatus of claim 9, wherein the first and second output terminals include a plurality of main electrode areas of each such transistor.

11. A photoelectric conversion apparatus of claim 8, further including:
means for connecting together the first output terminals of at least the plurality of cells exposed to light.

12. A photoelectric conversion apparatus of claim 11, wherein the calculation performing means performs a calculation between a signal obtained via the connecting means and a signal at one output terminal of the cell shielded from light.

13. A photoelectric conversion apparatus of claim 8, wherein the calculation performing means includes substracting means.

14. A photoelectric converter, comprising
a first transistor means responsive to light to store in a control electrode region thereof a number of charge carriers dependent on the received light,
a second transistor means similar to the first, but shielded from light, and
means for producing a signal which is a function of the difference in the numbers of charges stored in the control electrode regions of the first and second transistor means.

FIG. 1A

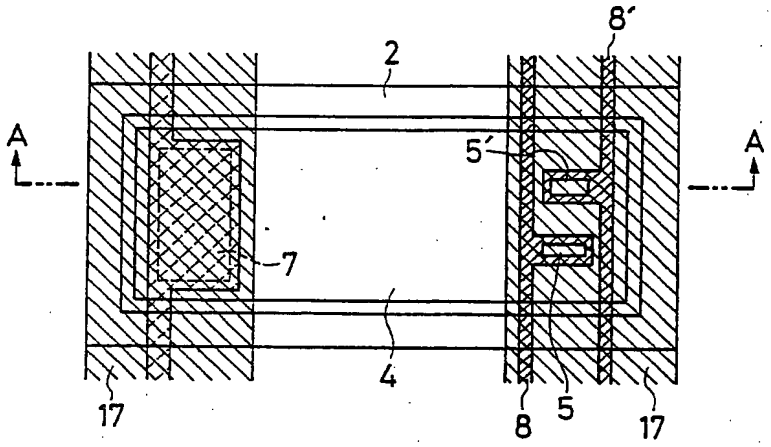


FIG. 1B

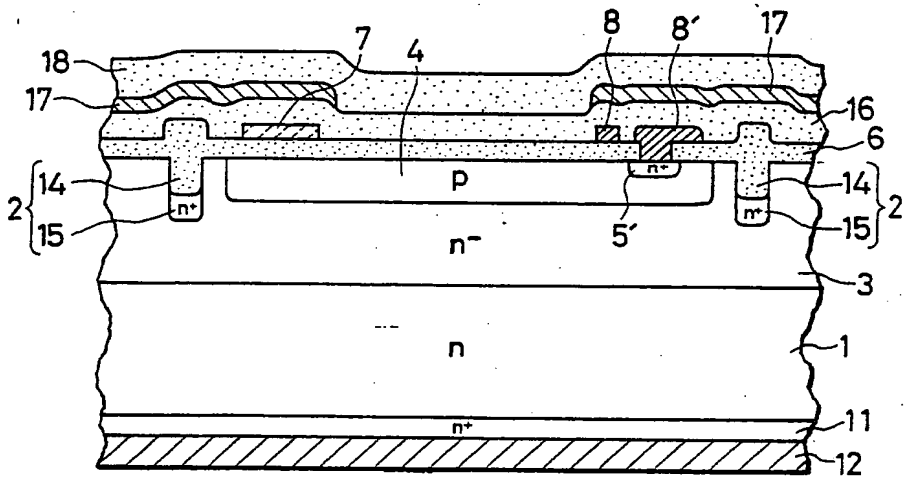


FIG. 1C

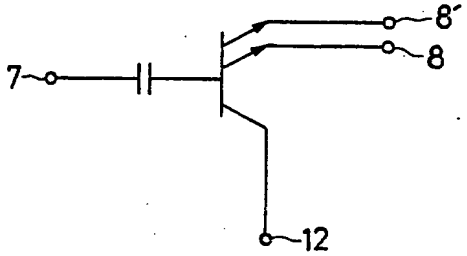


FIG. 2

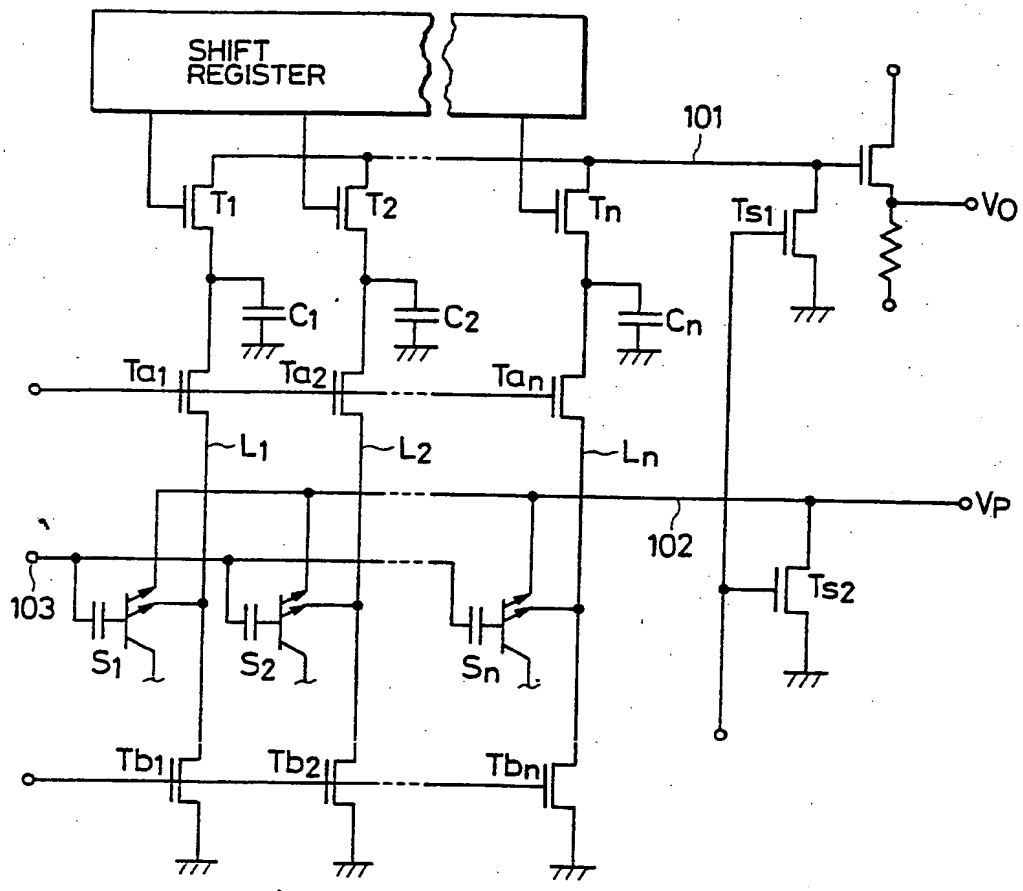

SHIFT REGISTER
101
T1
T2
Tn
Ts1
VO
C1
C2
Cn
Ta1
Ta2
Tan
L1
L2
Ln
VP
102
103
Ts2
S1
S2
Sn
Tb1
Tb2
Tbn

FIG. 3A

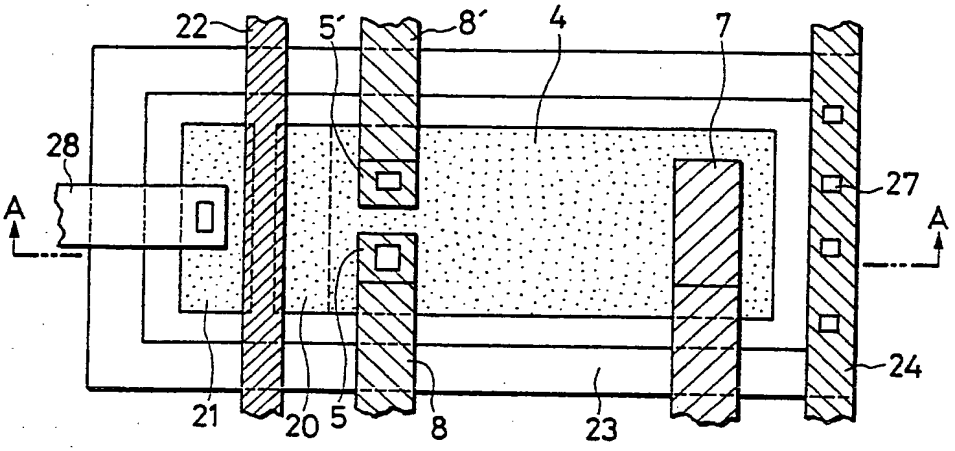


FIG. 3B

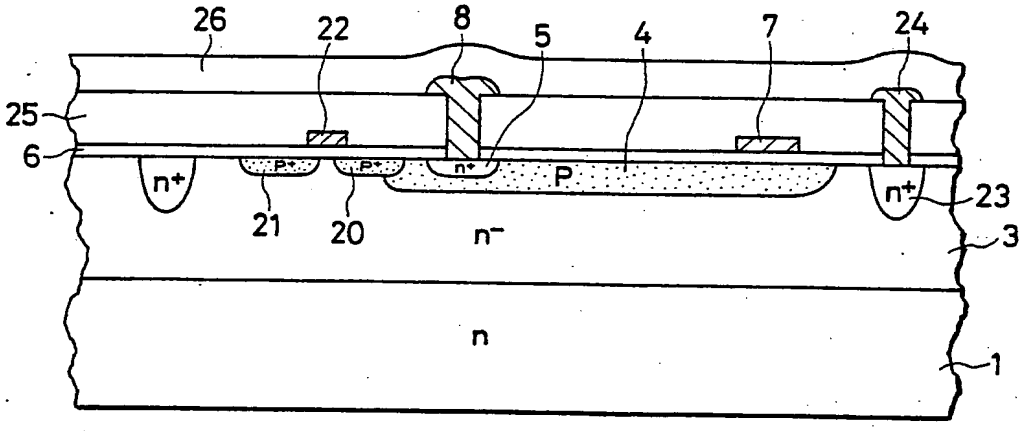


FIG. 3C

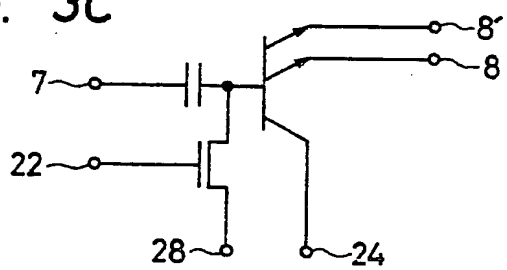


FIG. 4

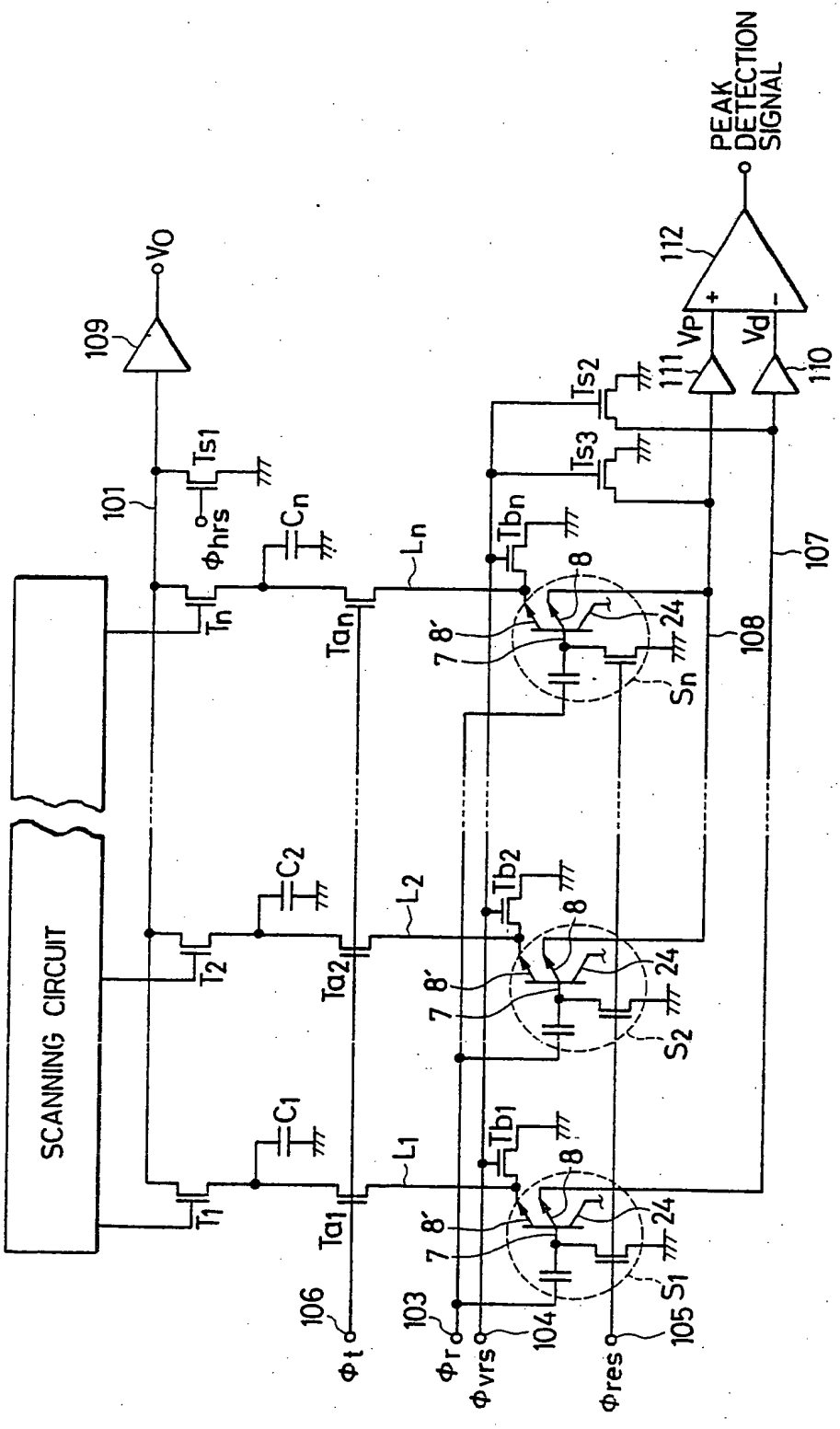
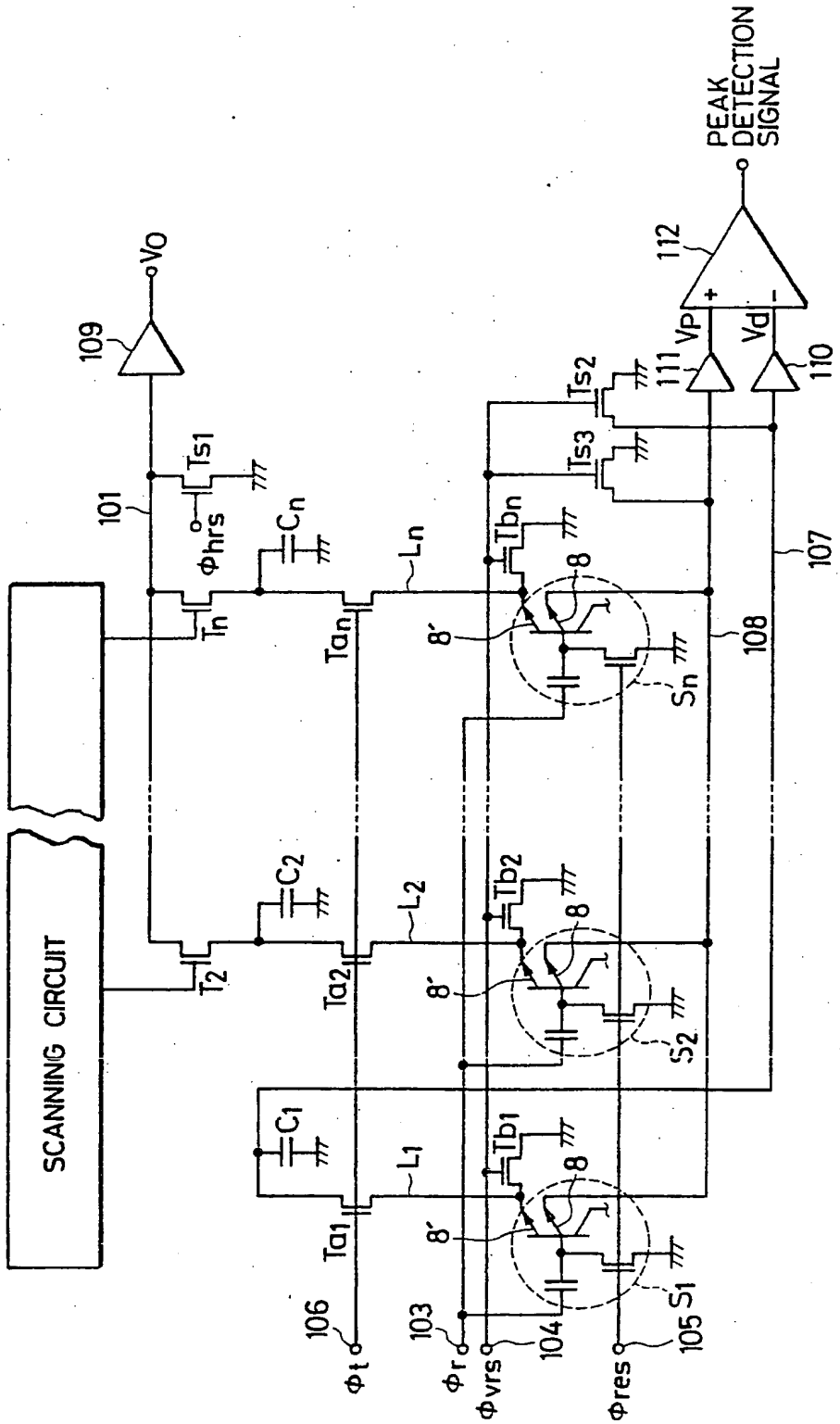

SCANNING CIRCUIT
PEAK DETECTION SIGNAL
VO
109
112
VP
Vd
111
110
101
107
108
Ts1
Ts2
Ts3
Φhrs
Cn
Ln
Tn
Tan
Tbn
Sn
C2
L2
T2
Ta2
Tb2
S2
C1
L1
T1
Ta1
Tb1
S1
7
8'
8
24
106
103
104
105
Φt
Φr
Φvrs
Φres

FIG. 5


SCANNING CIRCUIT
PEAK DETECTION SIGNAL
Vo
109
112
VP
Vd
111
110
101
107
108
Ts1
Ts2
Ts3
Φhrs
Cn
Ln
Tn
Tan
Tbn
Sn
C2
L2
T2
Ta2
Tb2
S2
C1
L1
Ta1
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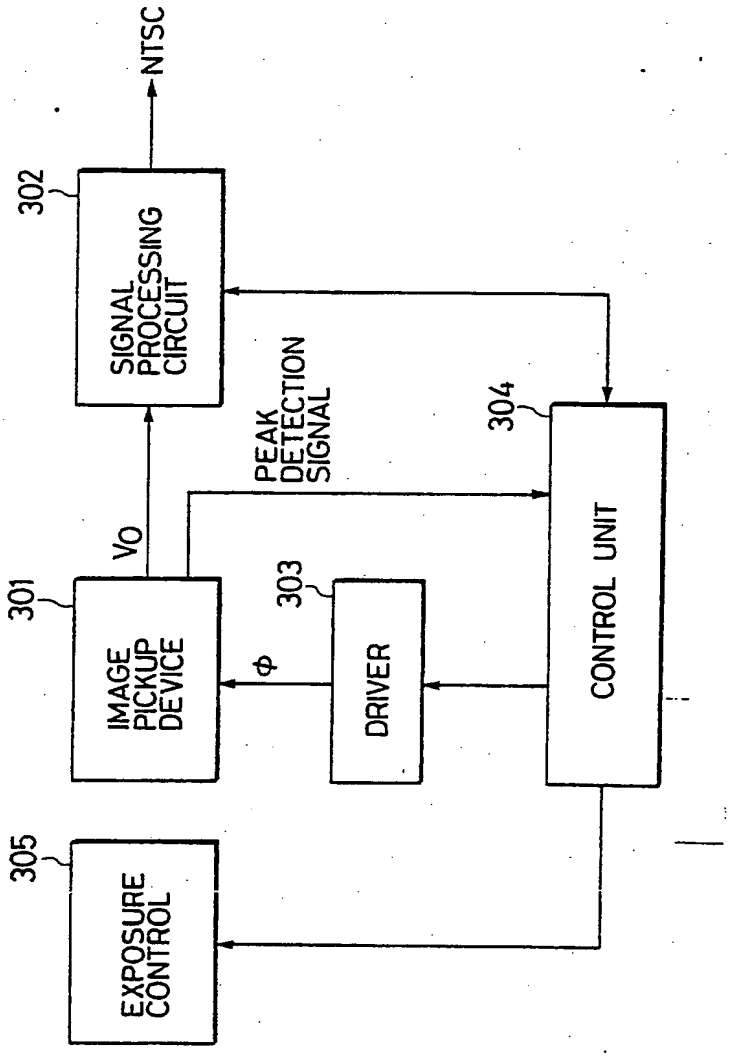
S1
8
8'
106
103
104
105
Φt
Φr
Φvrs
Φres

FIG. 6


NTSC
302
SIGNAL PROCESSING CIRCUIT
PEAK DETECTION SIGNAL
304
CONTROL UNIT
VO
301
IMAGE PICKUP DEVICE
303
DRIVER
Φ
305
EXPOSURE CONTROL

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 260 858**
A3

(12) # EUROPEAN PATENT APPLICATION

(21) Application number: 87307897.6

(51) Int. Cl.4: H01L 31/10 , H01L 27/14

(22) Date of filing: 07.09.87

(30) Priority: 19.09.86 JP 219668/86

(43) Date of publication of application:
23.03.88 Bulletin 88/12

(84) Designated Contracting States:
DE FR GB IT NL

(88) Date of deferred publication of the search report:
29.03.89 Bulletin 89/13

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(54) **Photoelectric conversion apparatus.**

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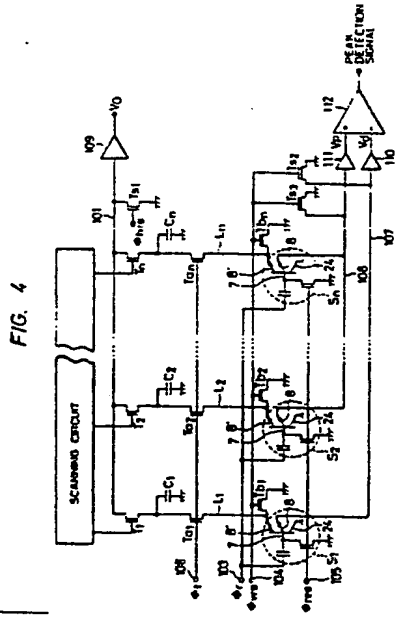

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 87 30 7897

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
Y	EP-A-0 132 076 (OHNI et al.) * Page 110, line 21 - page 114, line 17; claims; figure 23 *	1,3,4	H 01 L 31/10 H 01 L 27/14
P,Y D	EP-A-0 226 338 (CANON K.K.) * Whole document *	1,3,4	
Y	US-A-4 455 574 (HASHIMOTO et al.) * Column 1, lines 31-68; claims *	1,3,4	
X		8,11-14	
A	US-A-4 300 163 (WADA et al.) * Column 2, lines 9-35; claims *	1,8,11-14	
A	US-A-3 946 151 (KAMIYAMA et al.) * Column 3, lines 10-51 *	1,8,11-14	
A	GB-A-1 169 663 (COMMISARIAT A L'ENERGIE ATOMIQUE) * Page 1, lines 10-43; claims; figures 1-3 *	1,2,3	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H 01 L
H 04 N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12-01-1989	LINA F.

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